

January 24, 2005
Case No. PIIB 34,365 (7790/234)
Serial No.: 09/614,154
Filed: July 11, 2000
Page 2 of 10

CLAIM LISTING

A listing of the entire set of 1-13 is submitted herewith per 37 C.F.R. §1.121. This listing of claims 1-13 will replace all prior versions, and listings, of claims in the application.

1.-8. (Cancelled)

9. (Previously Presented) An active matrix array device, comprising:
- a substrate;
 - an array of individually addressable matrix elements carried on said substrate;
 - a set of address conductors connected to said array of matrix elements and carried on said substrate, said set of address conductors being arranged in a series of groups with each group including successive address conductors; and
 - an addressing circuit including
 - a multiplexing circuit integrated on said substrate and connected to said set of address conductors, said multiplexing circuit including a plurality of signal bus lines, said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines, and
 - a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate.
10. (Previously Presented) The active matrix array device of claim 9, wherein said signal processing circuits are arranged in series in a line parallel to said multiplexing circuit.

January 24, 2005
Case No. PHB 34,365 (7790/234)
Serial No.: 09/614,154
Filed: July 11, 2000
Page 3 of 10

11. (Previously Presented) The active matrix array device of claim 9, wherein a first subset of said signal processing circuits are arranged in a first row and a second subset of said signal processing circuits are arranged in a second row and offset from the first row in a brick-like fashion.

12. (Presently Presented) The active matrix array device of claim 9, wherein an order in which said signal processing circuits are arranged physically on said substrate is different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected.

13. (Previously Presented) An active matrix array device, comprising:
a substrate;
an array of individually addressable matrix elements carried on said substrate;
a set of address conductors connected to said array of matrix elements and carried on said substrate, said set of address conductors being arranged in a series of groups with each group including successive address conductors; and
an addressing circuit including
a multiplexing circuit integrated on said substrate and connected to said set of address conductors, said multiplexing circuit including a plurality of signal bus lines, said multiplexing circuit being arranged to couple sequentially each group of said set of address conductors to said plurality of signal bus lines with each address conductor in a group being coupled to a respective one of said signal bus lines, and
a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein an order in which said signal processing circuits are arranged physically on said substrate is at least partially different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected.